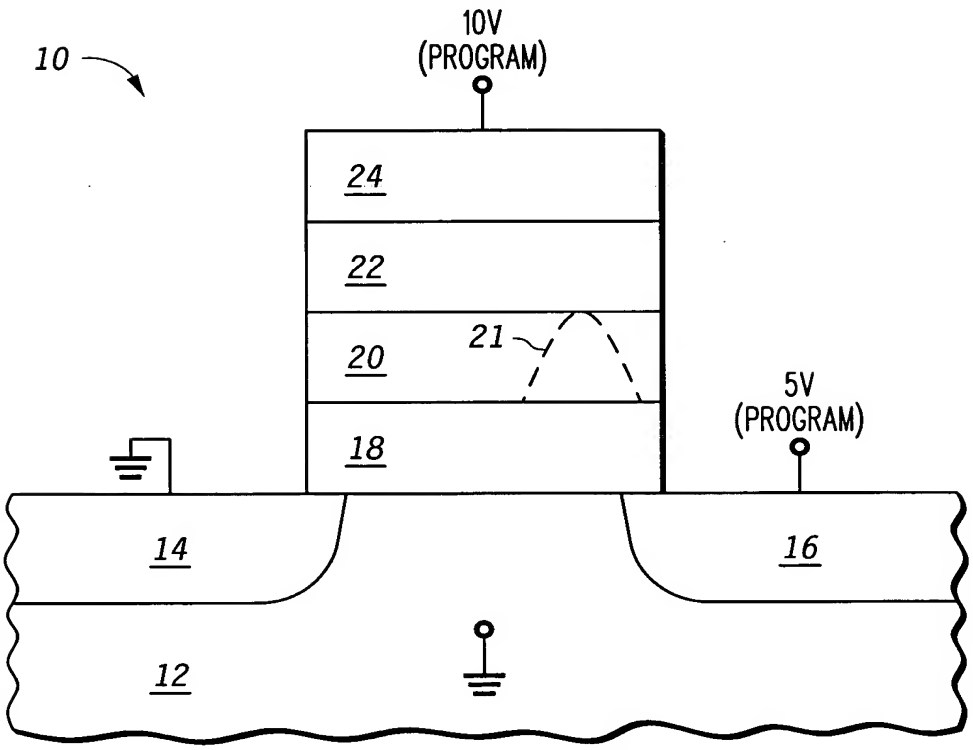


FIG. 1
-PRIOR ART-

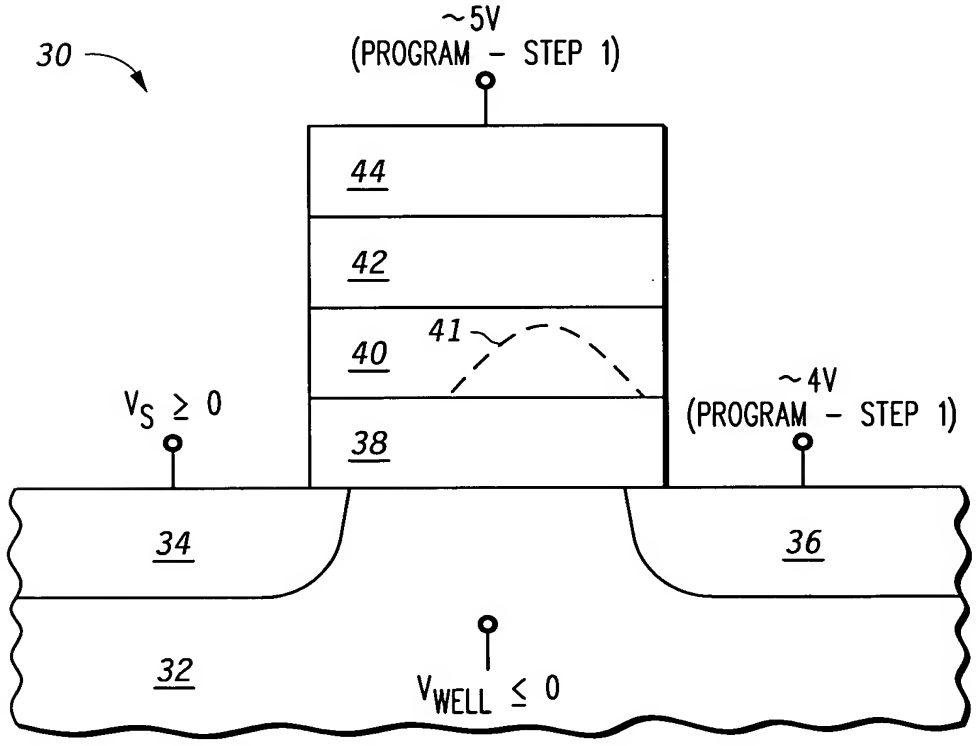


FIG. 2

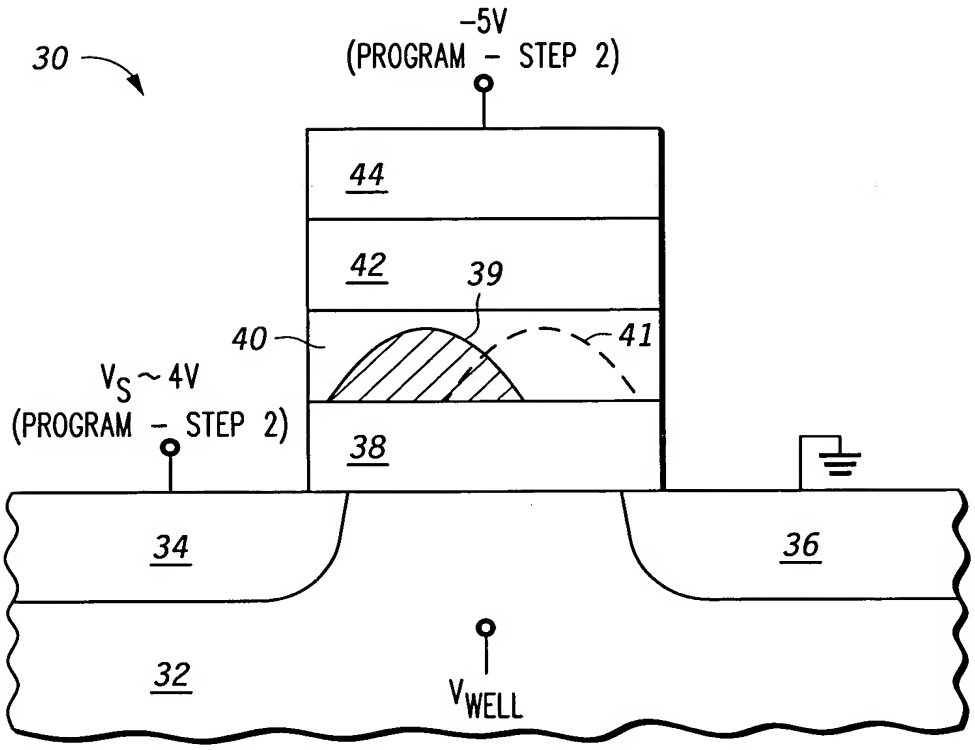
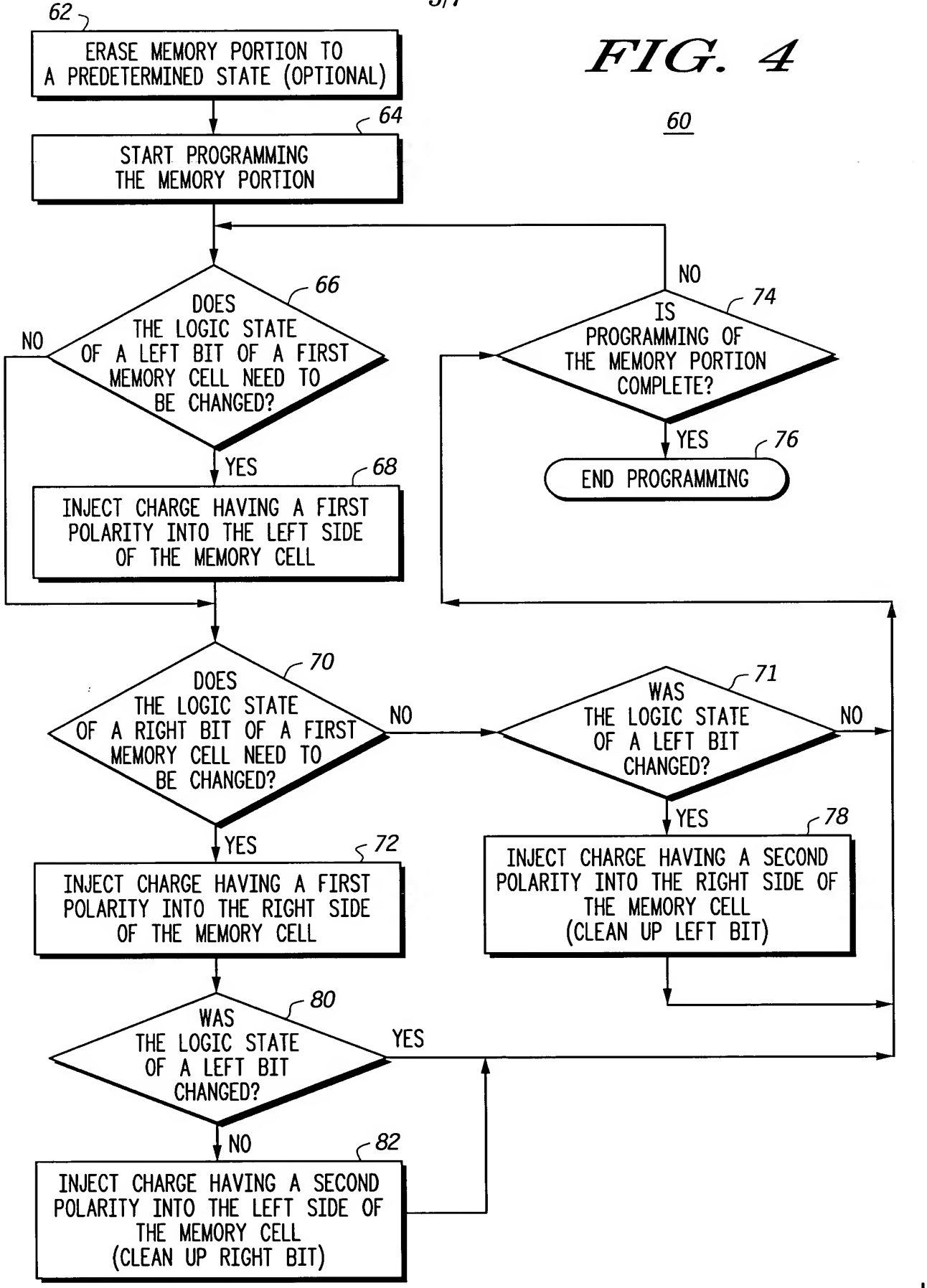

30
-5V
(PROGRAM - STEP 2)
44
42
39
40
41
$V_S \sim 4V$
(PROGRAM - STEP 2)
38
34
36
32
V_{WELL}

FIG. 3

FIG. 4


60
62
ERASE MEMORY PORTION TO A PREDETERMINED STATE (OPTIONAL)
64
START PROGRAMMING THE MEMORY PORTION
66
DOES THE LOGIC STATE OF A LEFT BIT OF A FIRST MEMORY CELL NEED TO BE CHANGED?
NO
YES
68
INJECT CHARGE HAVING A FIRST POLARITY INTO THE LEFT SIDE OF THE MEMORY CELL
70
DOES THE LOGIC STATE OF A RIGHT BIT OF A FIRST MEMORY CELL NEED TO BE CHANGED?
NO
YES
72
INJECT CHARGE HAVING A FIRST POLARITY INTO THE RIGHT SIDE OF THE MEMORY CELL
80
WAS THE LOGIC STATE OF A LEFT BIT CHANGED?
YES
NO
82
INJECT CHARGE HAVING A SECOND POLARITY INTO THE LEFT SIDE OF THE MEMORY CELL (CLEAN UP RIGHT BIT)
74
IS PROGRAMMING OF THE MEMORY PORTION COMPLETE?
NO
YES
76
END PROGRAMMING
71
WAS THE LOGIC STATE OF A LEFT BIT CHANGED?
NO
YES
78
INJECT CHARGE HAVING A SECOND POLARITY INTO THE RIGHT SIDE OF THE MEMORY CELL (CLEAN UP LEFT BIT)

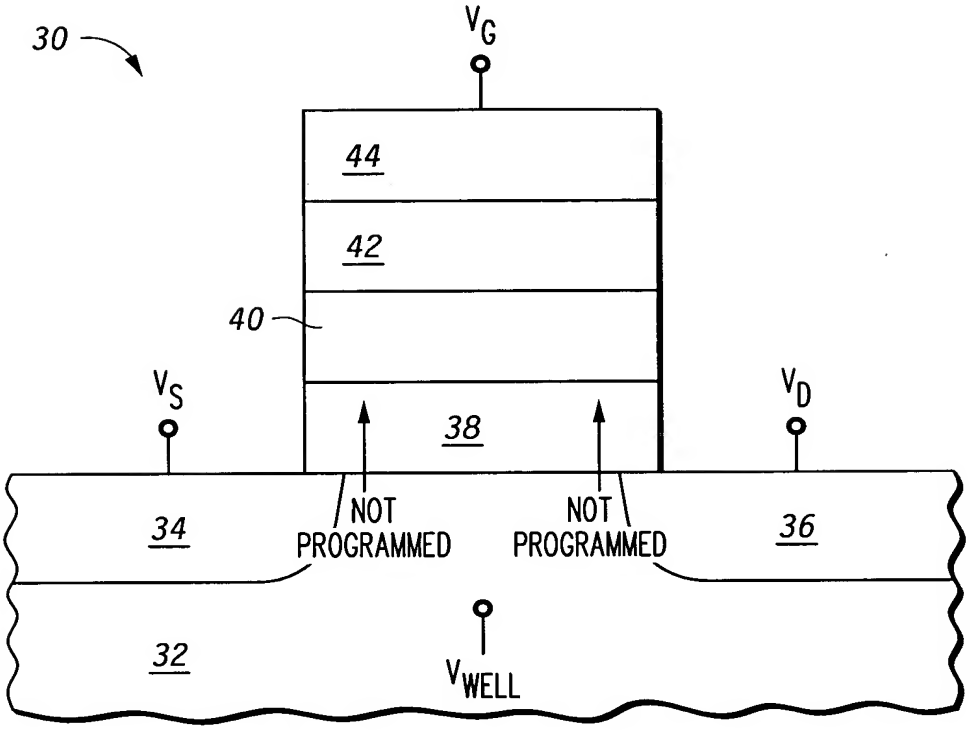

30
V_G
44
42
40
V_S
38
V_D
34
NOT PROGRAMMED
NOT PROGRAMMED
36
32
V_{WELL}

FIG. 5

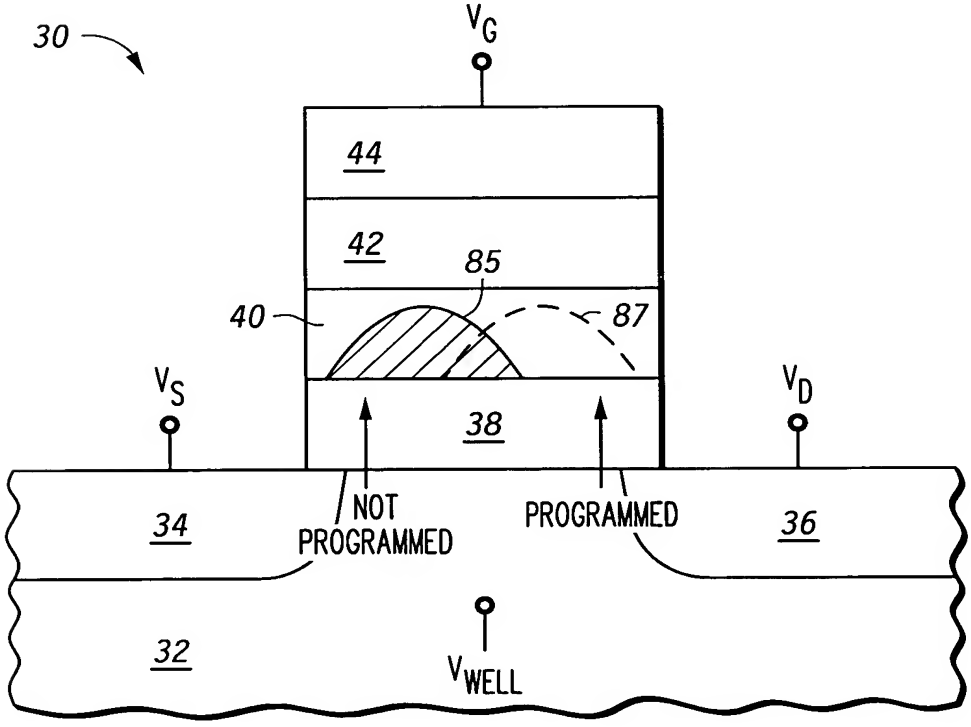

30
V_G
44
42
85
40
87
V_S
38
V_D
34
NOT PROGRAMMED
PROGRAMMED
36
32
V_{WELL}

FIG. 6

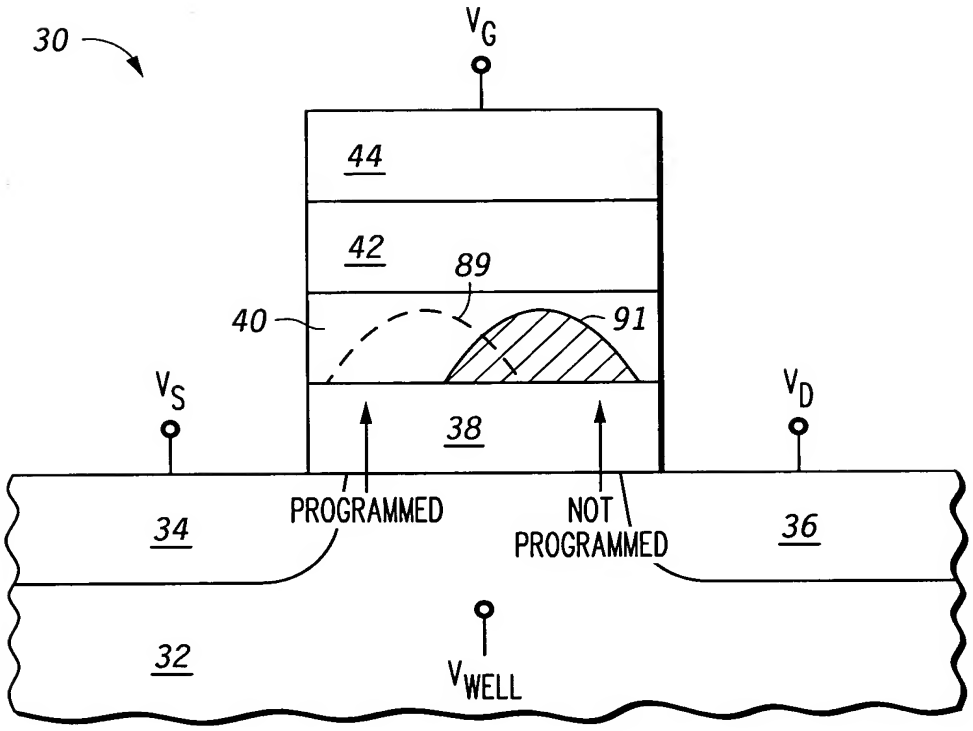

30
V_G
44
42
89
40
91
V_S
V_D
38
34
PROGRAMMED
NOT
PROGRAMMED
36
32
V_{WELL}

FIG. 7

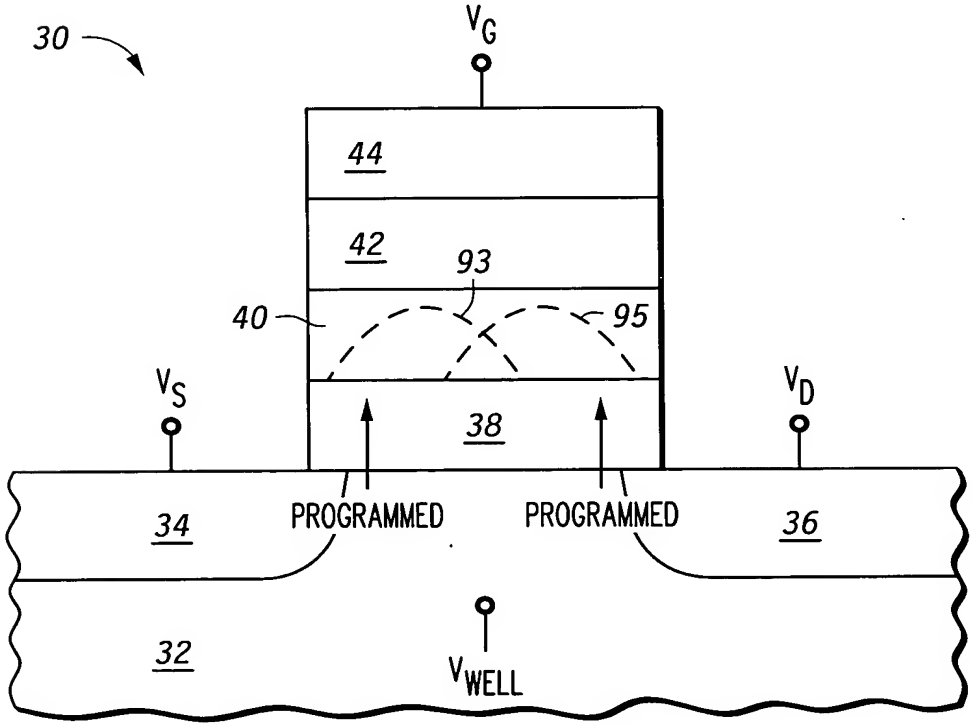

30
V_G
44
42
93
40
95
V_S
V_D
38
34
PROGRAMMED
PROGRAMMED
36
32
V_{WELL}

FIG. 8

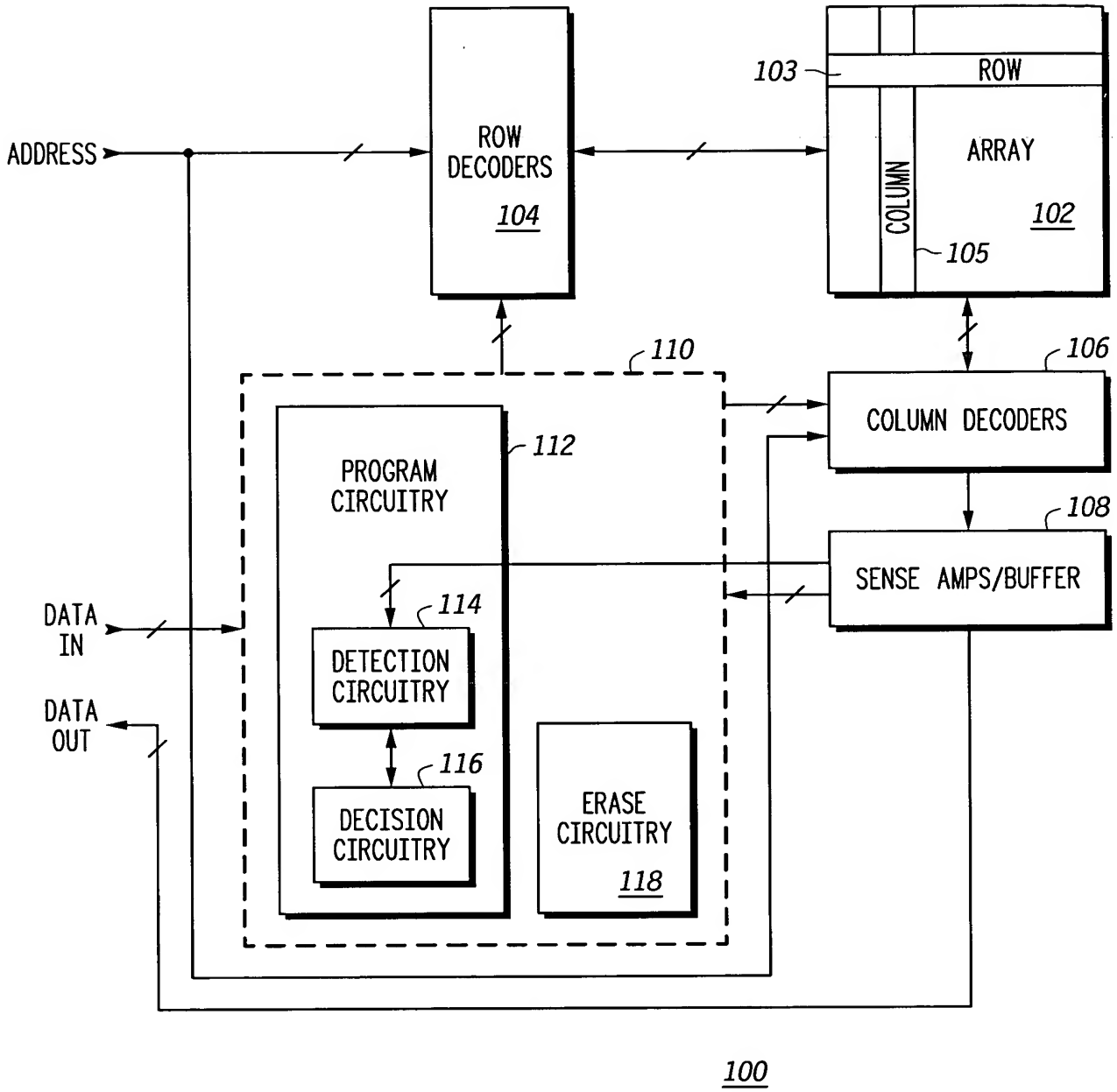

ADDRESS
ROW DECODERS
104
103
ROW
ARRAY
102
COLUMN
105
110
106
COLUMN DECODERS
PROGRAM CIRCUITRY
112
108
SENSE AMPS/BUFFER
DATA IN
DATA OUT
114
DETECTION CIRCUITRY
116
DECISION CIRCUITRY
ERASE CIRCUITRY
118
100

FIG. 9

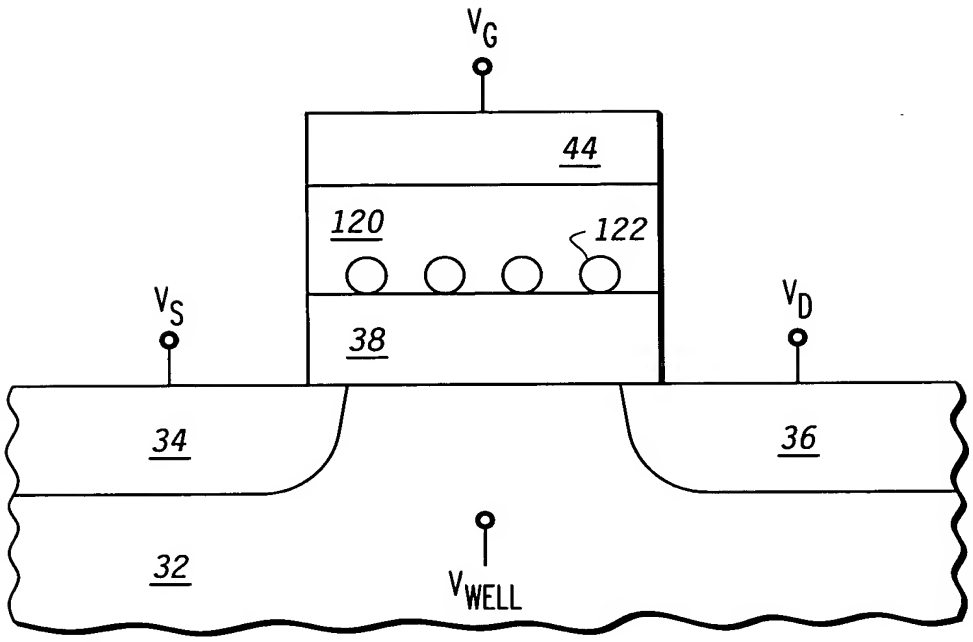

V_G
44
120
122
V_S
38
V_D
34
36
32
V_{WELL}

FIG. 10

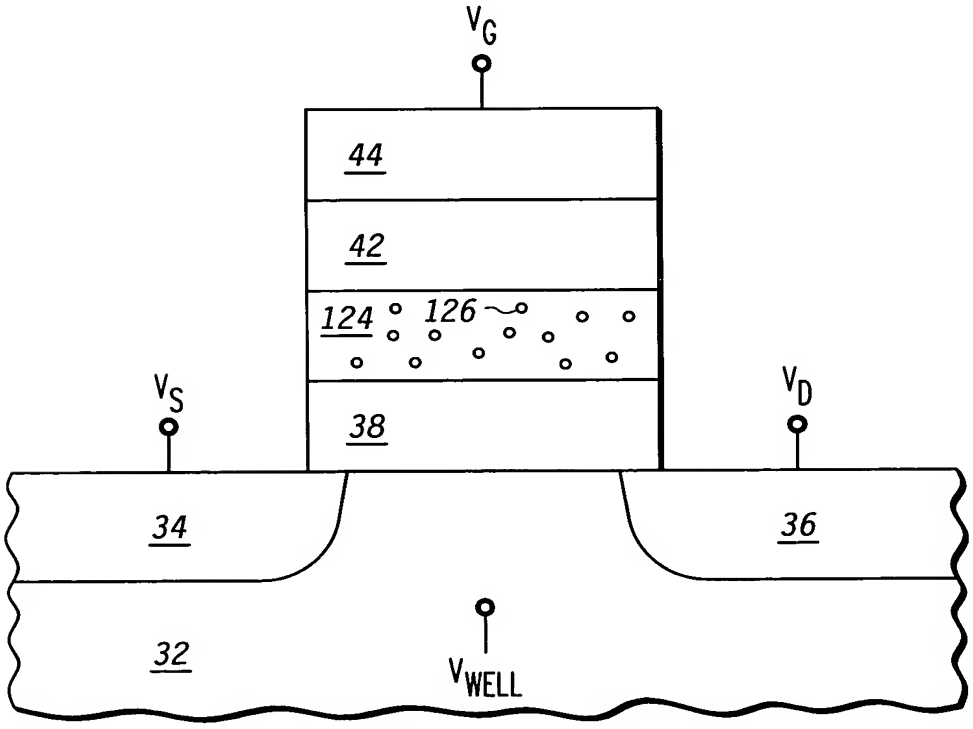

V_G
44
42
124
126
V_S
38
V_D
34
36
32
V_{WELL}

FIG. 11